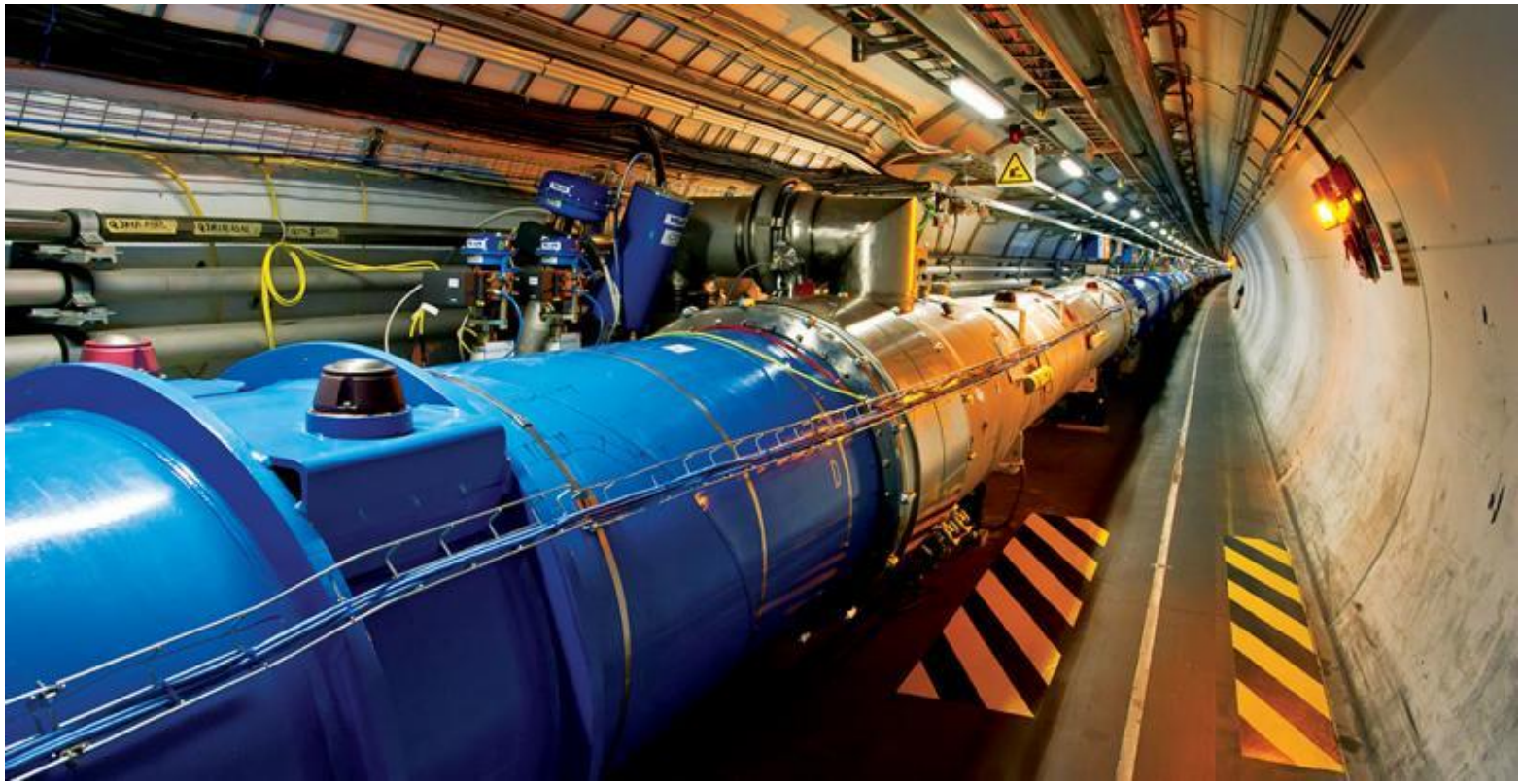

High DR ADC for LHC

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Last updated: 06/22/17

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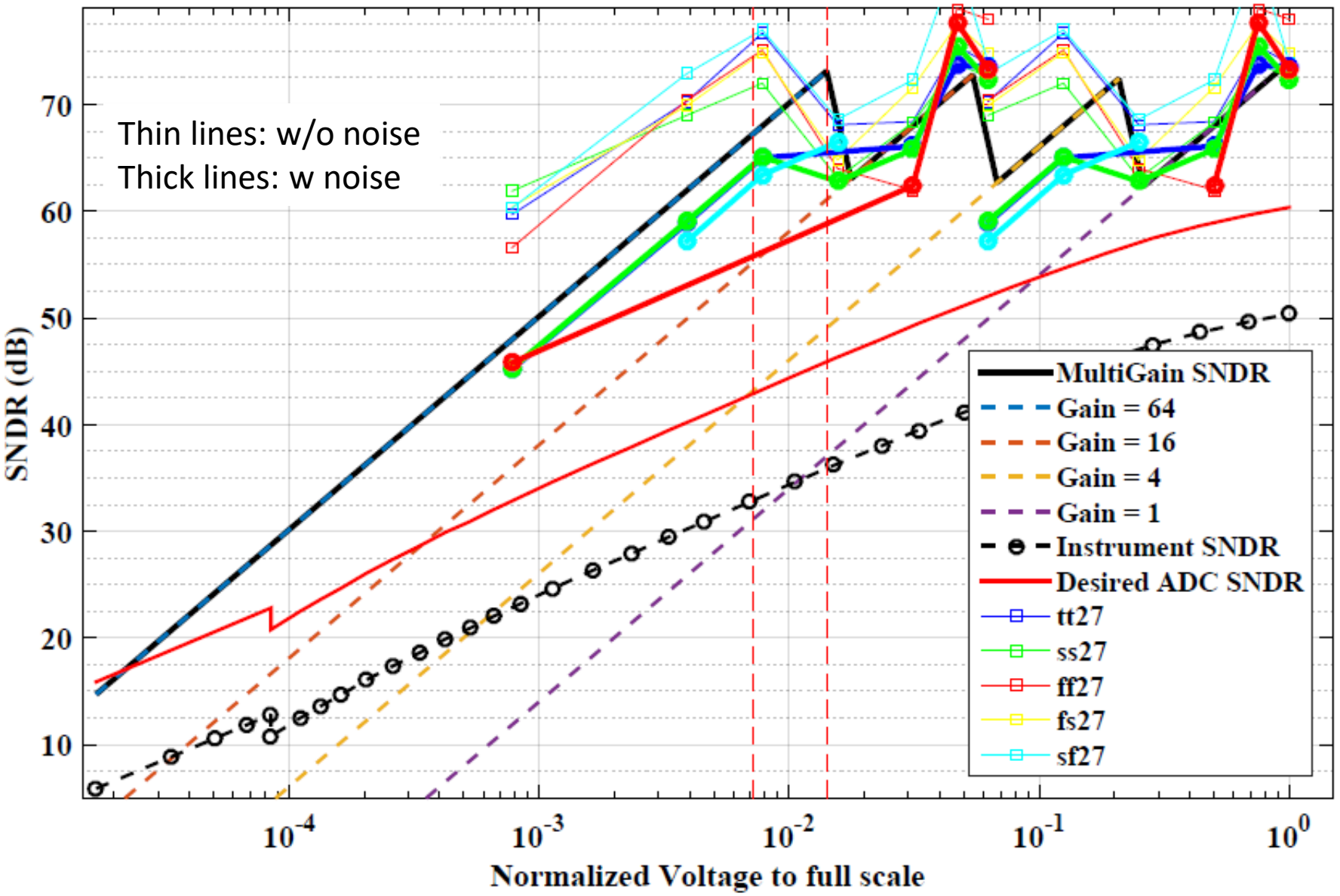
Simulation results update

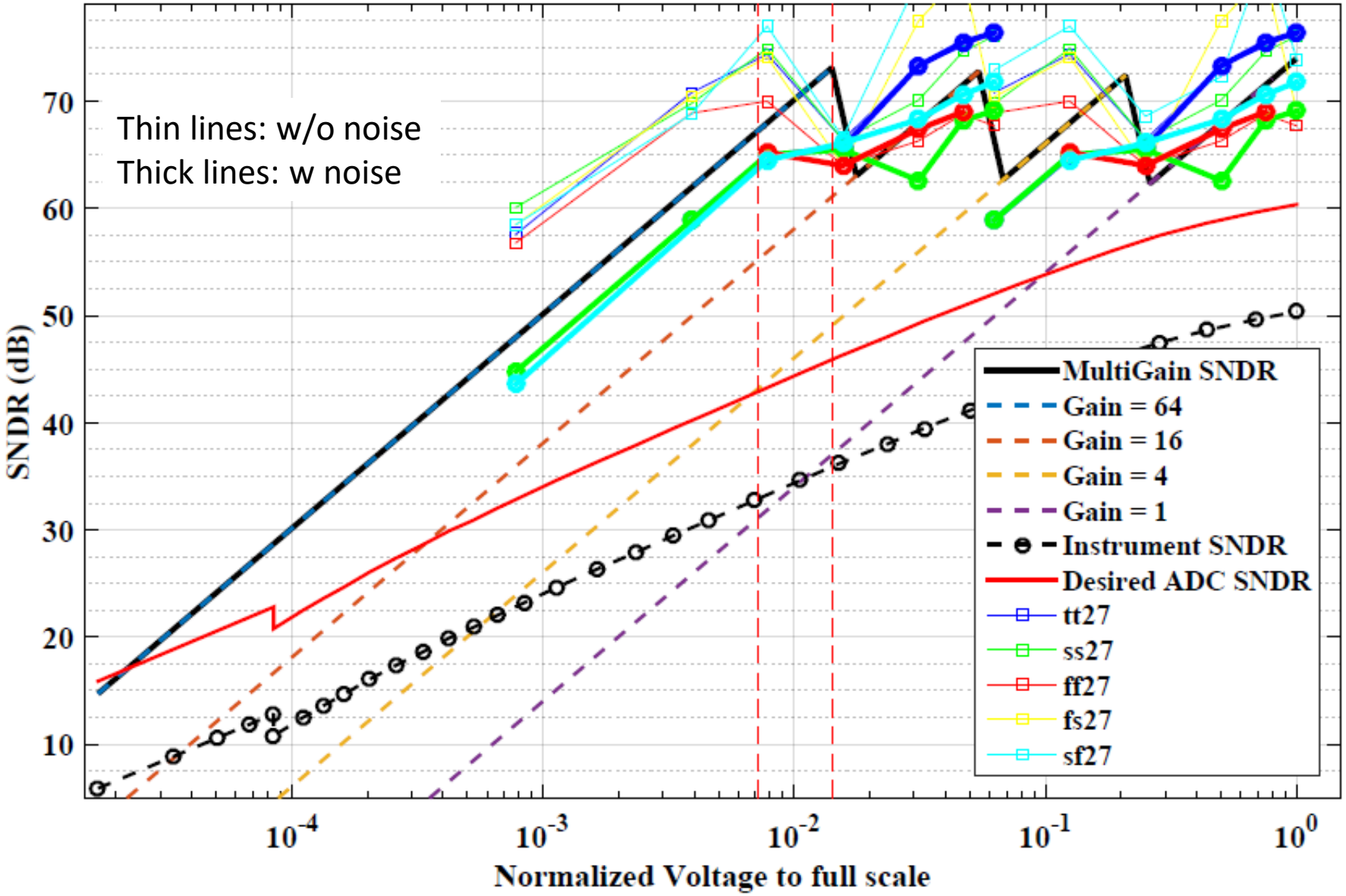
- For the DRE block, CERN requirements are currently met across corners for 27^{o}C.
- Below results are for top level chip simulations, with single scan chain setting, without bond wire and with noise and without noise.
- When noise is enabled, Fmin = 10kHz, Fmax = 2GHz

NOTE: Simulations for noise do not converge always. Results are provided for the cases when convergence was achieved.

Current SNDR plot: 4.375MHz input



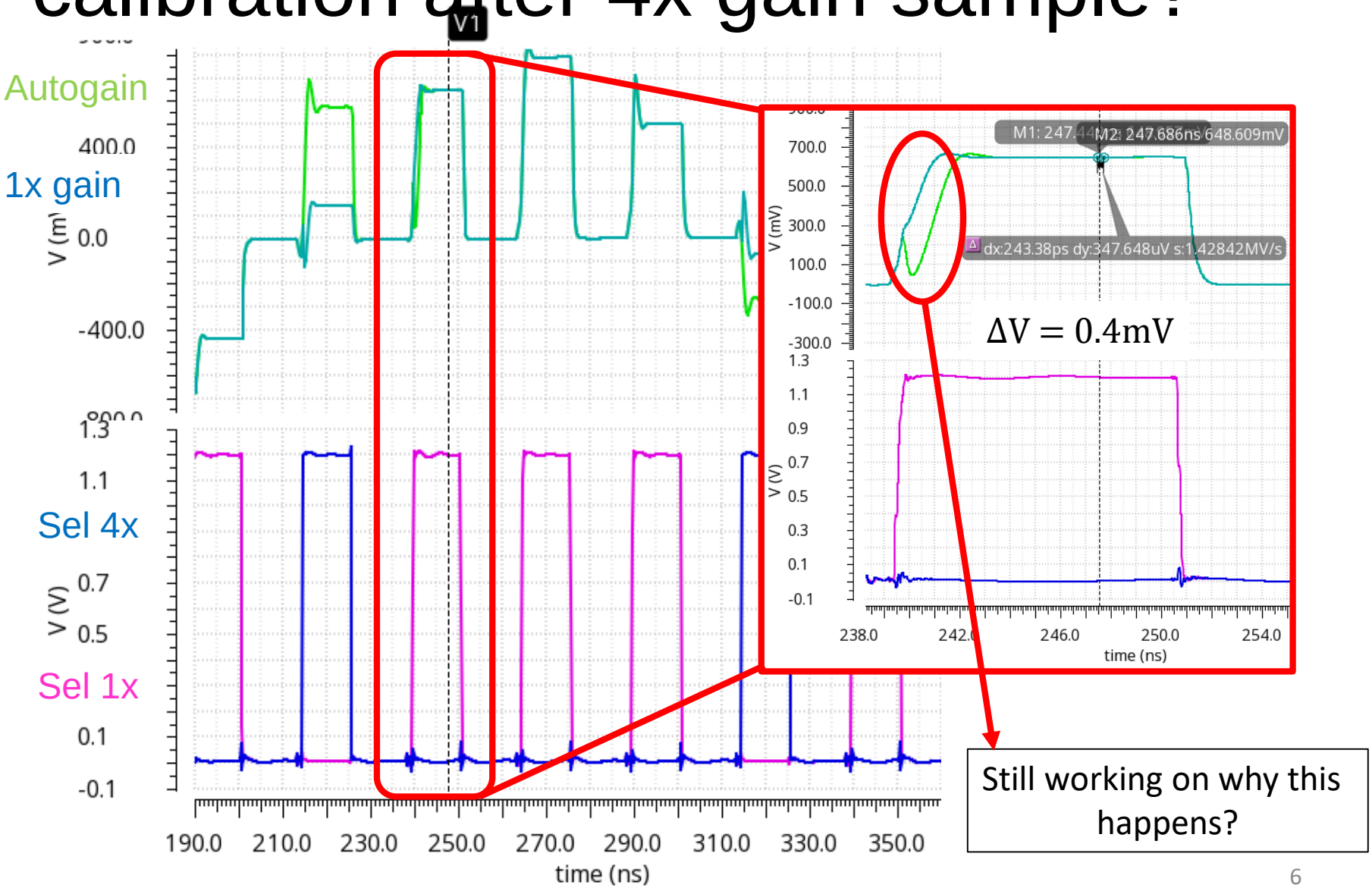
Current SNDR plot: 19.375MHz input



Why ff27 corner was not giving correct results earlier?

- Calibration requirement: Gain factor required = 3.95 instead of 4.
- Additional calibration enhances performance from 65dB to 69dB:
  - 1x Samples following 4x gain samples should be scaled up slightly.
  - Not sure why this problem happens. Work in progress (details on next slide)

Why 1x gain sample needs calibration after 4x gain sample?



Still working on why this happens?

Calibration factors used

Corner	4x Calibration Constant	1x Calibration Constant
tt 27	4	1
ss 27	3.99	0.9999
ff 27	3.95	0.999
fs 27	3.99	1
sf 27	3.999	1

- Normalized output sample value =
  - Vout (if gain = 1x, prev sample gain = 1x)
  - Vout/(1x Calib Const) (if gain = 1x, prev sample gain = 4x)
  - Vout/(4x Calib Const) (if gain = 4x)

Next steps

- Figure out:
  - How to find calibration constants?
    - Sine input or forcing 1x and 4x?
    - Tricky part is to find scaling factors for 1x following 4x.
  - Why is 1x calibration constant required? Can we eliminate the problem?
- Work on front end software for PCB interface.

Backup Slides

DRE Simulation Results

- Simulation done at top schematic level containing the whole chip with DRE analog output taken. Bondwires not present. **Noise is not enabled**
- Vfs = 1.6Vpp for DRE, 2Vpp for SAR. I = 18mA to 22mA

Input Freq	Input Amp (diffpp)	Ideal SNDR (for current architecture)	CERN SNDR required (including 10dB margin)	tt27 (3.99, 1)	ss27 (3.99, 0.9999)	ff27 (3.95, 0.999)	fs27 (3.99, 1)	sf27 (3.999, 1)
4.375M	1.6V	73dB	>60dB	73.83	72.6	77.93	74.9	73.85
No noise	1.2V	73dB	>59dB	75.46	73.8	79.04	77.5	83.86
	0.8V	73dB	>58dB	68.39	68.3	62.02	71.63	72.26
	0.4V	73dB	>54dB	68.06	63.13	63.95	64.83	68.65
	0.2V	67dB	>52dB	76.7	71.96	75.07	74.85	77.0
	0.1V	61dB	>52dB	70.3	68.98	70.37	69.85	72.9
	0.02V	47dB	(switches to 2nd gain)	59.7	61.86	56.63	60.41	60.25

(Self note: Sims: I13 on e4, I16 on e3, Chip_testbench)

(Coloring from CERN perspective)

DRE Simulation Results

- Simulation done at top schematic level containing the whole chip with DRE analog output taken. Bondwires not present. **Noise is enabled**
- Vfs = 1.6Vpp for DRE, 2Vpp for SAR. I = 18mA to 22mA

Input Freq	Input Amp (diffpp)	Ideal SNDR (for current architecture)	CERN SNDR required (including 10dB margin)	tt27 (3.99, 1)	ss27 (3.99, 1)	ff27 (3.95, 0.999)	fs27 (3.99, 1)	sf27 (3.999, 1)
4.375M	1.6V	73dB	>60dB	73.47	72.32	73.26	-	
With noise	1.2V	73dB	>59dB	73.7	75.5	77.7	-	-
	0.8V	73dB	>58dB	66.1	65.83	62.41	-	-
	0.4V	73dB	>54dB	-	62.83	-	-	66.54
	0.2V	67dB	>52dB	65.0	65.11	-	-	63.37
	0.1V	61dB	>52dB	58.86	59.11	-	-	57.15
	0.02V	47dB	(switches to 2nd gain)	45.19	45.3	45.76	-	-

(Self note: Sims: I13 on e4, I16 on e3, Chip_testbench)

(Coloring from CERN perspective)

DRE Simulation Results

- Simulation done at top schematic level containing the whole chip with DRE analog output taken. Bondwires not present. **Noise is not enabled**
- Vfs = 1.6Vpp for DRE, 2Vpp for SAR. I = 18mA to 22mA

Input Freq	Input Amp (diffpp)	Ideal SNDR (for current architecture)	CERN SNDR required (including 10dB margin)	tt27 (3.99, 1)	ss27 (3.99, 1)	ff27 (3.95, 0.999)	fs27 (3.99, 1)	sf27 (3.999, 1)
19.375 M	1.6V	73dB	>60dB	76.38	76.1	67.65	68.98	82.1
No noise	1.2V	73dB	>59dB	75.1	74.6	68.76	81.9	81.9
	0.8V	73dB	>58dB	73.27	70.1	66.32	77.46	81.4
	0.4V	73dB	>54dB	66.28	66.38	63.97	64.01	66.61
	0.2V	67dB	>52dB	74.4	74.93	70.01	74.14	76.95
	0.1V	61dB	>52dB	70.75	69.84	68.85	70.37	68.82
	0.02V	47dB	(switches to 2nd gain)	57.54	60.97	56.81	58.54	58.5

(Self note: Sims: I13 on e4, I16 on e3, Chip_testbench)

(Coloring from CERN perspective)

DRE Simulation Results

- Simulation done at top schematic level containing the whole chip with DRE analog output taken. Bondwires not present. **Noise is enabled**
- Vfs = 1.6Vpp for DRE, 2Vpp for SAR. I = 18mA to 22mA

Input Freq	Input Amp (diffpp)	Ideal SNDR (for current architecture)	CERN SNDR required (including 10dB margin)	tt27 (3.99, 1)	ss27 (3.99, 1)	ff27 (3.95, 0.999)	fs27 (3.99, 1)	sf27 (3.999, 1)
19.375 M	1.6V	73dB	>60dB	76.38	69.11	-	-	71.8
With noise	1.2V	73dB	>59dB	75.5	68.18	69.0	-	70.6
	0.8V	73dB	>58dB	73.27	62.6	67.4	-	68.3
	0.4V	73dB	>54dB	65.71	65.48	63.97	-	66.13
	0.2V	67dB	>52dB	64.94	64.97	65.24	-	64.47
	0.1V	61dB	>52dB	58.89	58.89	-	-	-
	0.02V	47dB	(switches to 2nd gain)	-	44.75	-	-	43.62

(Self note: Sims: I13 on e4, I16 on e3, Chip_testbench)

(Coloring from CERN perspective)